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EXHIBIT 2

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TOSHIBA CORPORATION, Plaintiff, v. LEXAR MEDIA, INC., Defendant.

No. C 03-0167 MJJ

UNITED STATES DISTRICT COURT FOR THE NORTHERN DISTRICT OF CALIFORNIA

2005 U.S. Dist. LEXIS 5213

January 24, 2005, Decided
January 24, 2005, Filed

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JUDGES: MARTIN J. JENKINS, UNITED STATES DISTRICT JUDGE.

OPINIONBY: MARTIN J. JENKINS

OPINION:

CLAIM CONSTRUCTION ORDER

INTRODUCTION

Before the Court are the parties' proposed constructions of several disputed terms contained in nine of Toshiba Corporation's patents. Having carefully read and considered the parties' briefs, the arguments proffered by the parties at the November 22, 2004 claim construction hearing, and the parties' supplemental briefs, the Court construes the disputed claim terms as follows.

FACTUAL BACKGROUND

The nine patents-in-suit are generally directed to non-volatile semiconductor memory technology. Six of the patents at issue relate to flash [*2] memory products having a memory controller and flash memory such as CompactFlash(R) cards. These are *U.S. Patent Number 5,546,351* ("the 351 patent") entitled "Non-Volatile Semiconductor Memory Device and Memory System Using the Same;" *U.S. Patent Number 5,611,067* ("the 067 patent") entitled "Non-Volatile Semiconductor Memory Device Having Means For Selective Transfer of Memory Block Contents and For Chaining Together Unused Memory Blocks;" *U.S. Patent Number 5,724,300* ("the 300 patent") entitled "Non-Volatile Semiconductor Memory Device and Memory System Using the Same;" *U.S. Patent Number 5,793,696* ("the 696 patent") entitled "Non-Volatile Semiconductor Memory Device and Memory System Using the Same;" *U.S. Patent Number 5,946,231* ("the 231 patent") entitled "Non-volatile Semiconductor Memory Device;" and *U.S. Patent Number 5,986,933* ("the 933 patent") entitled "Semiconductor Memory Device Having Variable Number of Selected Cell Pages and Subcell Arrays."

The three other patents-in-suit relate to memory card readers. These patents are *U.S. Patent Number 6,094,697* ("the 697 patent") entitled "Information Processing System Including Processing Device for Detecting Non-Conductivity [*3] of State-Indicating Non-Conductive Member and Discriminating Prohibit State of Writing Information to Information Writable Storage Medium;" *U.S. Patent Number 6,292,850* ("the 850 patent") entitled "Information Storage System Including State-Designating Area on Memory Card and Detecting Presence or Absence of State-Designating Member on State-Designating Area to Inhibit or Allow Writing of Information;" and *U.S. Patent Number 6,338,104* ("the 104 patent") entitled "System Including Single Connector Pin Supporter Having Two Separate Plurality of Connector Pins With One Set of Pins Contacting State Designating Portion of Memory Card Indicating Write Prohibit State."

The parties initially identified twenty-two disputed claim terms to be construed by the Court. However, because Lexar conceded to the construction of several of these terms, and because some of the disputed claim terms appear in patents that share a common disclosure such that the common terms are to be construed consistently (*see*

Legal Standard discussion *infra*), only 14 disputed claim terms remain for the Court's construction. Six of these are means-plus-function claims in which the parties only dispute what constitutes [*4] the corresponding structure.

DISPUTED CLAIM TERMS

The following is a list of the disputed claim terms construed in this Order:

. "page" in the *351* and *696* patents;

. "page" in the *933 patent*;

. "order" in the *067 patent*;

. "simultaneously" in the *351* and *696 patents*;

. "simultaneously" in the *933 patent*;

. "collective verify signal" in the *351 patent*;

. "control unit" in the *231 patent*;

. "memory controller" in the *850/'104 patents*;

. "memory means" in the *351 patent*;

. "memory means" in the *067 patent*;

. "erasing means" in the *067 patent*;

. "control means" in the *067 patent*;

. "managing means" in the *067 patent*; and

. "means for informing" in the *067 patent*.

LEGAL STANDARD

The construction of a patent claim is a matter of law for the Court. *Markman v. Westview Instruments, Inc., 517 U.S. 370, 372, 134 L. Ed. 2d 577, 116 S. Ct. 1384 (1996)*. The Court must conduct an independent analysis of the disputed claim terms. It is insufficient for the Court to simply choose between the constructions proposed by the adversarial parties. *Exxon Chem. Patents v. Lubrizol Corp., 64 F.3d 1553, 1555 (Fed. Cir. 1995)*. [*5] "The subjective intent of the inventor when he used a particular term is of little or no probative weight in determining the scope of a claim (except as documented in the prosecution history)." *Markman v. Westview Instruments, Inc., 52 F.3d 967, 985 (Fed. Cir. 1995)* (*en banc*), *aff'd, Markman, 517 U.S. 370, 134 L. Ed. 2d 577, 116 S. Ct. 1384*. "Rather the focus is on the objective test of what one of ordinary skill in the art at the time of the invention would have understood the term to mean." *Id. at 986*. To determine the meaning of a patent claim, the Court considers three sources: the claims, the specification, and the prosecution history. *Id. at 979*.

The Court looks first to the words of the claims. *Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576, 1582 (Fed. Cir. 1996)*. "Although words in a claim are generally given their ordinary and customary meaning, a patentee may choose to be his own lexicographer and use terms in a manner other than their ordinary meaning, as long as the special definition of the term is clearly stated in the patent specification or file history." *Id.* (citation omitted). "A technical term used in a patent document is interpreted [*6] as having the meaning that it would be given by persons experienced in the field of the invention, unless it is apparent from the patent and the prosecution history that the inventor used the term with a different meaning." *Hoechst Celanese Corp. v. BP Chems. Ltd., 78 F.3d 1575, 1578 (Fed. Cir. 1996)*. The doctrine of claim differentiation creates the presumption that limitations stated in dependent claims are not to be read into the independent claim from which they depend because different language used in separate claims is presumed to indicate that the claims have different meanings and scope. *Tandon Corp. v. U.S. International Trade Com., 831 F.2d 1017, 1023 (Fed. Cir. 1987)*.

Second, it is always necessary to review the specification to determine whether the inventor has used any terms in a manner inconsistent with their ordinary meaning. *Vitronics, 90 F.3d at 1582*. The specification can act as a dictionary when it expressly or impliedly defines terms used in the claims. *Id.* Because the specification must contain a description of the invention that is clear and complete enough to enable those of ordinary skill in the art to [*7] make and use it, the specification is the single best guide to the meaning of a disputed term. *Id.* The written description part of the specification itself does not delimit the right to exclude, however; that is the function and purpose of claims. *Markman, 52 F.3d at 980*.

Third, the court may consider the prosecution history. *Vitronics, 90 F.3d at 1582*. "Although the prosecution history can and should be used to understand the language used in the claims, it too cannot enlarge, diminish, or vary the limitations in the claims." *Markman, 52 F.3d at 980* (internal quotation marks deleted) (citations omitted). However, a concession made or position taken to establish patentability in view of prior art on which the examiner has relied, is a substantive position on the technology for which a patent is sought, and will generally generate an estoppel. In contrast, when claim changes or arguments are made in order to more particularly point out the applicant's invention, the purpose is to impart precision, not to overcome prior art. Such prosecution is not presumed to raise an estoppel, but is reviewed on its facts, with the guidance of [*8] precedent. *Pall Corp. v. Micron Separations, Inc., 66 F.3d 1211, 1220 (Fed. Cir. 1995)* (citations omitted).

Disputed claim terms are construed consistently across all claims within a patent. *Southwall Techs., Inc. v. Cardinal IG Co., 54 F.3d 1570, 1579 (Fed. Cir. 1995)*. Where patents-in-suit share the same disclosures, common terms are construed consistently across all claims in both patents. *Mycogen Plant Sci., Inc. v. Monsanto Co., 252 F.3d 1306, 1311 (Fed. Cir. 2001)* (*overruled on other grounds)*. Similarly, where two patents share common disclosures, common claim terms should be construed consistently. *Mycogen Plant Sci., Inc. v. Monsanto Co., 252 F.3d 1306, 1311 (Fed. Cir. 2001)*. Also, where multiple patents stem from the same parent application, the prosecution history of one is relevant to the construction of common claim terms. *Microsoft Corp. v. Multi-Tech Sys., 357 F.3d 1340, 1349 (Fed. Cir. 2004)*. However, common claim terms in patents stemming from the same parent application need not necessarily be construed consistently across patents. *MSM Invs. Co. LLC v. Carolwood Corp., 259 F.3d 1335 (Fed. Cir. 2001).* [*9]

Ordinarily, the Court should not rely on expert testimony to assist in claim construction, because the public is entitled to rely on the public record of the patentee's claim (as contained in the patent claim, the specification, and the prosecution history) to ascertain the scope of the claimed invention. *Vitronics, 90 F.3d at 1583*. "[W]here the public record unambiguously describes the scope of the patented invention, reliance on any extrinsic evidence is improper." *Id.* Extrinsic evidence should be used only if needed to assist in determining the meaning or scope of technical terms in the claims, and may not be used to vary or contradict the terms of the claims. *Id.* (quoting *Pall Corp., 66 F.3d at 1216*); *Markman, 52 F.3d at 981*.

The Court is free to consult technical treatises and dictionaries at any time, however, in order to better understand the underlying technology and may also rely on dictionary definitions when construing claim terms, so long as the dictionary definition does not contradict any definition found in or ascertained by a reading of the patent documents. *Vitronics, 90 F.3d at 1584 n.6*. [*10] The Court also has the discretion to admit and rely upon prior art proffered by one of the parties, whether or not cited in the specification or the file history, but only when the meaning of the disputed terms cannot be ascertained from a careful reading of the public record. *Id. at 1584*. Referring to prior art may make it unnecessary to rely on expert testimony, because prior art may be indicative of what all those skilled in the art generally believe a certain term means. *Id.* Unlike expert testimony, these sources are accessible to the public prior to litigation to aid in determining the scope of an invention. *Id.*

In the case at bar, the parties seek the Court's construction of six claims that they agree are means-plus-function claims. A means-plus-function claim is a special type of patent claim described in *35 U.S.C. section 112,* paragraph 6, which provides:

> An element in a claim for a combination may be expressed as a means or a step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, [*11] or acts described in the specification and equivalents thereof.

35 U.S.C. § 112, P 6. Under this provision, an inventor can describe an element of the invention by the result accomplished or the function served, rather than by describing the item or element to be used. *Warner-Jenkinson Co., Inc. v. Hilton Davis Chemical Co., 520 U.S. 17, 27, 137 L. Ed. 2d 146, 117 S. Ct. 1040 (1997)*. When using means-plus-function language, "[t]he applicant must describe in the patent specification some structure which performs the specified function." *Valmont Industries, Inc. v. Reinke Mfg. Co., Inc., 983 F.2d 1039, 1042 (Fed. Cir. 1993)*. A structure disclosed in the specification is only deemed to be "the corresponding structure" if the specification clearly links or associates that structure to the function recited in the claim. *Kahn v. GMC, 135 F.3d 1472, 1476 (Fed. Cir. 1998)*. The duty to link or associate structure in the specification with the function is the *quid pro quo* for the convenience of employing the means-plus-function format. *Id.*

An accused device with a structure that is not identical to the structure described [*12] in the patent will literally infringe the patent if the accused device performs the identical function required by the means-plus-function claim with a structure identical or equivalent to that described in the patent. *Cybor Corp. v. FAS Technologies, Inc., 138 F.3d 1448, 1457 (Fed. Cir. 1998)* (en banc); *Kahn, 135 F.3d at 1476*. "Thus, the statutory provision prevents an overly broad construction by requiring reference to the specification, and at the same time precludes an overly narrow construction that would restrict coverage solely to those means *expressly* disclosed in the specification." *Symbol Technologies, Inc. v. Opticon, Inc., 935 F.2d 1569, 1575 (Fed. Cir. 1991)* (citations omitted).

Claim construction of a means-plus-function limitation involves two steps: first, the Court must identify the claimed function; second, the Court must determine the corresponding structure described in the specification necessary to perform that function *Tex. Digital Sys. v. Telegenix, Inc., 308 F.3d 1193, 1208 (Fed. Cir. 2002)* (citation omitted).

ANALYSIS

As a threshold matter, the Court notes that the *351*, *696*, [*13] and *300 patents* share a common specification such that claim terms common to those patents (e.g. "page" and "simultaneously") will be construed consistently. The *697*, *850*, and *104 patents* also share a common specification such that the claim phrase "memory controller," the only claim term to be construed in these patents, will be construed consistently across those patents.

I. "page" in the *351/'696 patent*

Lexar's proposed construction:	Toshiba's proposed construction:
the unit of data, consisting of 256 bytes, programmed to and read from the memory at the memory at the same time	the unit of data, consisting of a plurality of bytes, written to and read from the same time

Claims 4 and 5 of the *351* recite writing pages into memory and claim 2 of the *696* recites programming pages into memory. The parties' dispute over the proper construction of the term is twofold: first, the parties disagree about whether a page, in the *351/'696* is limited to 256 bytes; and second, the parties disagree about whether a page is "written to" or "programmed to." The Court addresses each of these disputes in turn.

Lexar contends that a page, by definition, consists [*14] of 256 bytes. According to Lexar, the *351* and *696* specifications require such a limitation even though the claim language itself says nothing about page size. Indeed, both portions of the *351* specification cited by Lexar (column 24, lines 56–57 and column 32, lines 46–49), which describe preferred embodiments, teach 256 bytes per page. Column 24, lines 56–57 describes the preferred embodiment as exemplified by Figure 57 in which the EEPROM has "a structure of 256 bytes per one page." Similarly, column 32, lines 46–49 suggests that in the preferred embodiment described, a page consists of 256 bytes. The same holds true for the portions of the *696* specification cited by Lexar. The language describing preferred embodiments in column 35, lines 43–46 and in column 36, lines 52–53 of the *696*, describing a page as 256 bytes.

Toshiba argues that nothing in the *351/'696* claim language or the specifications limits a page to 256 bytes. Generally, a limitation from a preferred embodiment cannot be imported into the construction of a claim term. *Markman, 52 F.3d at 980*. However, Lexar contends that the consistent use of a 256–byte page in the specification means that under [*15] *Alloc, Inc. v. ITC, 342 F.3d 1361, 1368 (Fed. Cir. 2003)*, the claim itself is so limited. The Court finds, however, that this argument is unavailing here. Here, the patent specifications' references to a 256–byte page (two references per specification) do not rise to the level described in *Alloc* of "mak[ing] clear . . . that the claimed invention is narrower than the claim language might imply." *Id. at 1370*. In *Alloc*, everything in the specification led to the unavoidable conclusion that "the invention as a whole, not merely a preferred embodiment, provides for play in the positioning of floor panels.'" *Id. at 1368–69*. The court in *Alloc* also noted that the patent specification specifically criticized prior art floor systems without "play," strongly suggesting that the invention required it. Here, on the other hand, the Summary of the Invention sections of the *351* and the *696* patents say nothing about the size of a page, nor do the Abstracts. Moreover, there are only four references to 256–byte pages in the two patents. Additionally, the patents do not criticize prior art for using pages of other [*16] sizes. The Court finds that the references to 256–byte pages in the *351* and *696* patent specifications do not rise to the level of consistent usage dictating a limitation in the construction of the term. Therefore, because the claim language does not limit a page to 256 bytes and because the specification does not clearly and consistently narrow a page to 256 bytes, the Court rejects this portion of Lexar's proposed construction.

With regard to the parties' dispute over whether a page is written to or programmed to, Lexar contends that Toshiba's proposed construction is too broad because "writing" encompasses both programming and erasing. Lexar argues that limiting a page to that which is "programmed to" is more precise. "Program" is defined as "the operation of injecting electrons onto the floating gate of the memory cell." (IEEE FGA Standard Definitions at 23.) Lexar acknowledges the IEEE's definition of a page as "a section of an array that may be written to simultaneously." Lexar goes on to argue, however, that based on the specification and prosecution history, "page" must be further limited to that which is "programmed to" rather than "written to." Toshiba, for its part, only [*17] spends a few sentences in its Opening Brief (and no effort in its Reply) on the programming/writing dispute. Toshiba contends that the language of the *933*'s specification supports its construction but the Court declines to look to a wholly unrelated patent to construe a common claim term.

For these reasons, "page" in the *351*/'*696* is construed as *the unit of data, consisting of a plurality of bytes, programmed to and read from the memory at the same time.*

II. "page" in the *933 patent*

Lexar's proposed construction:	Toshiba's proposed construction:
the unit of data, consisting of 256 bytes, programmed to and read from the memory the memory at the same time	the unit of data, consisting of a plurality of bytes, written to and read from at the same time

The dispute here is the same. The parties propose the same respective constructions of "page" in the *933 patent* that they propose for the *351*/'*696 patent* and again, their dispute is focused on the size of a page and on whether a page is "programmed to" or "written to" the memory. At oral argument, Lexar and Toshiba reported that they agree that "page" in the *933* should be construed consistently [*18] with its construction in the *351*/'*696*. However, the parties' agreement in that regard does not bind the Court. Because the *933 patent* is wholly unrelated to the *351* and the *696 patents*, the Court engages in a separate analysis of the disputed claim term here.

Here, unlike in the *351*/'*696* discussion *supra*, the parties' references to the *933* specification are relevant. Claims 1, 4, 31, and 34 of the *933* recite writing pages into memory. Lexar again urges the Court to find that a "page" is limited to 256 bytes. Nothing in the claims themselves restricts a page to 256 bytes. Therefore, Lexar relies on the specification language describing a preferred embodiment to support its proposed construction. Generally, as discussed *supra*, limitations from a preferred embodiment cannot be imported into the claims. *Markman, 52 F.3d at 980*. However, Lexar contends that the consistent reference to a 256-byte page in the *933 patent* specification means that under *Alloc, 342 F.3d at 1368*, the claim term itself is so limited.

Lexar's *Alloc* argument is somewhat more compelling in the context of the *933 patent*. In the *933*, the specification frequently [*19] refers to a page of 256 bytes. (*See, e.g.*, *933 patent* 9:43-46.) However, the specification also frequently refers to memory cell pages without any reference to their size. (*See, e.g.*, *933 patent* 3:20-24, 3:38-40, 3:56-58.) This is at odds with *Alloc* where a narrower construction was only deemed appropriate where the limitation was made clearly and consistently throughout the patent. *342 F.3d at 1368*. Moreover, the Summary of the Invention section also describes a page of 1024 bytes and "pages of different sizes." ('*933 patent* 10:42, 10:63, 11:48.) Lexar explains that these references correspond to the selection of multiple pages of 256 bytes each, not to single pages containing more than 256 bytes. However, the Court finds that the references to pages of different sizes preclude a finding that the specification's references to 256-byte pages rise to the level of "mak[ing it] clear . . . that the claimed invention is narrower than the claim language might imply, as described in *Alloc.* Therefore, the Court declines to limit the construction of "page" to 256 bytes.

With regard to the programming/writing dispute, Toshiba argues that the intrinsic evidence [*20] of the *933* describes only writing, rendering its proposed construction more consistent with the intrinsic evidence. Here, the Court agrees with Toshiba. The claim language of the independent claims (1 and 31) in the *933* teaches a semiconductor memory device containing a page in which "a read or write operation is performed." ('*933 patent* 15:24; *933 patent* 18:51-52.) Toshiba's citation to a portion of the specification, column 2, lines 4-5 and 12-13, in which the reading and writing of pages is described, does not further the inquiry, however, because that language appears in the background of the invention section and does not describe the invention itself. But the language cited by Toshiba at column 10, lines 9–29, is instructive because it appears in the preferred embodiment section. The language there describes the write and read operations performed to a page. Because it would be improper to construe a claim term to exclude a preferred embodiment of the invention and because, as Lexar itself points out, programming is, at least in some respects, a narrower process than writing, the Court cannot limit a "page" to be "programmed to" when a preferred embodiment teaches a page that [*21] is written to. Lexar argues that here that "writing" in the *933 patent* really means "programming," but the Court is unconvinced.

The Court construes "page" in the *933* as *the unit of data, consisting of a plurality of bytes, written to and read from the memory at the same time.*

III. "order" in the *067 patent*

Lexar's proposed construction:	Toshiba's proposed construction:
arrangement of linking in a chain by pointers	arrangement

The parties dispute the proper construction of "order" in claim 16 of the *067 patent*. n1 Claim 16 of the *067 patent* recites a memory system, including a nonvolatile semiconductor memory device, comprising a "control means for writing data to said unused blocks on the basis of an order in which said unused blocks are arranged." Toshiba contends that the term "order" here is used in its ordinary sense and should be construed simply as "arrangement." Lexar, on the other hand, argues that Toshiba's proposed construction does not add any value or clarity to the meaning of the claim term and that the construction of "order" should refer to a "chain" arrangement.

> n1 The Court notes that Toshiba objects to the inclusion of "order" in the list of claim terms to be construed. According to Toshiba, Lexar originally included the term in its list but removed it; the parties did not discuss the term in the meet and confer process associated with the Joint Claim Construction Statement ("JCCS") and did not include the term in the JCCS. Moreover, according to Toshiba, Lexar only provided its proposed construction of the term two days before Toshiba's opening claim construction brief was to be filed. Toshiba claims that it was prejudiced because it did not have sufficient time to analyze the term or to adequately consider and respond to Lexar's proposed construction. Lexar contends, however, that it listed "order" in its 4-1 disclosures, as required by the Patent Local Rules, and that Toshiba had adequate time to consider and respond, particularly since Lexar offered Toshiba extra time to file its opening brief. The Court finds that Toshiba had adequate time to analyze the term and consider Lexar's proposed construction such that it was not unduly prejudiced.

[*22]

Lexar argues that the specification of the *067* supports its proposed construction because various preferred embodiments teach a chain arrangement. Generally speaking, it is improper to import a limitation from the specification into the claim construction. *Markman, 52 F.3d at 980*. However, as discussed *supra*, the Federal Circuit has recently found that where the specification consistently and clearly uses a claim term in a specific way, the claim term may be so limited. *Alloc, 342 F.3d at 1368*. Here, though, only the third preferred embodiment, described in the Summary of the Invention section, references pointers. ('*067 patent* 3:35–55.) The other embodiments described contain no such reference. ('*067 patent* 2:40–45, 3:17–34.) Therefore, the rule announced in *Alloc* does not apply here and Lexar's construction cannot be right.

Moreover, Lexar's prosecution history argument is equally unavailing. As Toshiba explains, the excerpts of the file history cited by Lexar refer to claims in the *067* that are dependent from claim 16 in which a chain arrangement of unused blocks is expressly disclosed. The excerpts do not read on the construction of [*23] "order" in independent claim 16.

Furthermore, Toshiba contends that the doctrine of claim differentiation prohibits referring to a chain arrangement in the construction of "order" in claim 16. Indeed, claim 17, dependent from claim 16, teaches a particular order of unused blocks in which the blocks are arranged in a chain. If the "order" in which the unused blocks, referenced in claim 16, are arranged the same way, there is no purpose for laying out the chain arrangement in claim 17. Elements recited in a dependent claim cannot be read into the broader, independent claim from which it depends. *Tandon Corp., 831 F.2d at 1023*. Therefore, Toshiba is right that "order" in claim 16 should not be limited to an arrangement of linking in a chain by pointers.

The Court finds, however, that Toshiba's proposed construction, "arrangement," is so simple as to fail to sufficiently explain what "order" means. "Arrangement" adds nothing to the understanding of "order" here. The Court notes that the term "order" refers to how the control means writes data to unused blocks. Therefore, the Court construes "order" in accordance with its ordinary meaning, but places it in the proper [*24] context of flash memory technology. "Order" is *a logical or comprehensible arrangement of unused blocks.*

IV. "simultaneously" in the *351/'696 patent*

Lexar's proposed construction:	Toshiba's proposed construction:
at the same time	at the same time without intentional delay

Claim 6, wherein "simultaneously" appears in the *351 patent*, reads as follows:

> The memory system of claim 1, wherein the memory cells are divided into a plurality of erase blocks each of said erase blocks are erased simultaneously, and a plurality of data groups are written in each of said erase blocks.
>
> "Simultaneously" appears in claim 7 of the *696 patent* as follows:
>
> The memory system according to claim 2, wherein the program termination detector simultaneously determines whether each data latch circuit stores the second logic level.

Lexar argues that the plain meaning of "simultaneously" is "at the same time," and that the Court should adopt this as the proper construction of the term. Lexar notes the Federal Circuit's finding in *Linear Technology Corp. v. Impala Linear Corp., 371 F.3d 1364 (Fed. Cir. 2004)*, that the plain meaning [*25] of the word "simultaneously," according to Webster's Third New International Dictionary, is "at the same time; concurrently." Lexar also contends that the *351* specification supports its construction in that it equates the term "simultaneously" with the language "at the same time." Indeed, column 2, lines 3–4 of the *351* says that "[i]n the erase operation, data in all memory cells within the NAND cell are erased at the same time."

Toshiba argues that the context of the claim language requires that the claim term be construed as "at the same time without intentional delay." Toshiba suggests that Lexar's proposed construction is overly broad and that Toshiba's proposed construction is better because it clarifies that it is the erasing that occurs simultaneously, not the condition of being erased that is simultaneous. However, Toshiba's argument relies on the specification of the *933*, unrelated to the *351* or the *696*. The Court declines to import limitations from one patent into the construction of a common claim term in a wholly unrelated patent. Moreover, however, Toshiba's proposed construction does not add anything substantive to the term's meaning. The Court finds that the [*26] ordinary meaning of the term, as offered by Lexar, is the proper construction. "Simultaneously" in the *351/'696* is therefore construed as *at the same time.*

V. "simultaneously" in the *933 patent*

Lexar's proposed construction:	Toshiba's proposed construction:

Lexar's proposed construction:	Toshiba's proposed construction:
at the same time	at the same time without intentional delay

Claims 1, 4, 15, 18, 31, and 34 of the *933 patent* employ the disputed claim term "simultaneously." The parties propose the same respective constructions of "simultaneously" in the *933 patent* that they proposed in the *351/'696 patent*. The Court looks first to the claim language itself. Claim 1 of the *933 patent* teaches:

A semiconductor memory device comprising:

> a memory cell array having a plurality of memory cells arranged in a matrix; and word lines, each word line being connected to plural memory cells and forming one page, wherein a number of pages selected simultaneously when a read or write operation is performed, is variable.

Claim 4, dependent from claim 1, teaches that "the number of pages selected simultaneously is varied by a command input from outside a chip." Claim 15 teaches a semiconductor memory device [*27] comprising a memory cell array with a plurality of sub-cell arrays, wherein "each of the sub-cell arrays includes a memory cell which is coupled to a word line and a bit line, a data circuit being coupled to the bit line, and a number of sub-cell arrays to be selected simultaneously is variable when a read or a write operation is performed." Claim 18, dependent from claim 15, teaches that the number of sub-cell arrays selected simultaneously is varied by a command input from outside a chip. Claim 31 teaches a semiconductor memory device comprising a memory cell array with a plurality of sub-cell arrays wherein each of the sub-cell arrays has at least one page respectively, and a number of pages selected from said plurality of sub-cell arrays simultaneously when a read or a write operation is performed, is variable. Claim 34, dependent from claim 31, teaches that "the number of pages selected simultaneously is varied by a command input from outside a chip."

Lexar, citing *Linear Technology Corp.*, argues that the ordinary meaning of the word "simultaneously" should be adopted as the proper construction of the term. *371 F.3d 1364* (the plain meaning of "simultaneously, [*28] " according to Webster's Third New International Dictionary, is "at the same time; concurrently"). Lexar contends that there is nothing about the claim language or the specification that suggests that the inventor intended a different meaning for the term and that, in fact, the specification supports adopting the ordinary meaning. Indeed, column 10, lines 42-43 explain that "[w]hen the page size is 1024 bytes, the sub-cell arrays A, B, C, and D are selected at the same time." This language appears in the Detailed Description of the Invention Section and strongly suggests that "simultaneously," as that term is used in claims 15, 18, and 31, means "at the same time." Similarly, column 10, lines 50-54 and 63-64 explain that pages are selected "at the same time." This language, also appearing in the section that describes the invention itself, suggests that "simultaneously," as that term is used in claims 1, 4, and 34, means "at the same time."

Toshiba argues that it is the selection of pages and sub-cell arrays that occurs simultaneously, "not the condition of being selected that is simultaneous." The Court agrees but does not find that Lexar's proposed construction suggests otherwise. [*29] Moreover, Toshiba's proposed language "without intentional delay" does not clarify the meaning of "simultaneously," but instead, as Lexar suggests, muddles its construction further.

The Court finds that Lexar's proposed construction is more appropriate here and construes "simultaneously" in accordance with its ordinary meaning. Simultaneously in the *933 patent* is therefore construed as *at the same time.*

VI. "collective verify signal" in the *351 patent*

Lexar's proposed construction:	Toshiba's proposed construction:
a signal output from the input /output buffer that is generated n2 upon the simultaneous verification of the state of a plurality of memory cells	n3 a signal that a collective verify operation has taken place. A "collective verify operation" is as imultaneous verification of the state of a plurality of memory cells

Lexar's proposed construction:	Toshiba's proposed construction:

n2 At oral argument, Lexar conceded that the word "simultaneous" could be employed in the construction rather than its initially proposed "parallel." (Claim Construction Transcript 31:6–13.)

n3 At oral argument, Toshiba conceded that the term "signal" could be employed in the construction rather than its initially proposed "indication." (Claim Construction Transcript 33:8–9.)

[*30]

The disputed claim phrase "collective verify signal" appears in claims 1, 4, and 5 of the *351 patent*. Claim 1 of the *351* teaches:

> a memory means having a plurality of memory cells . . . for outputting a collective verify signal when all the data of the data group have been written; and . . . said memory means to allow said memory means to latch and write the transferred new data group therein and further to transfer the collective verify signal to said control circuit whenever the new latched data group has been written.

Claim 4 teaches:

> a read only memory (ROM), said ROM configured to receive data of a predetermined number of bits as a page of data and to output a collective verify response to the collective verify signal received from said ROM, the control circuit outputs data to be next written to said ROM.

Claim 5 teaches:

> A memory system as recited in claim 4, wherein said ROM comprises an electrically erasable ROM (EEPROM) . . . wherein during the write operation for writing m pages of data into the EEPROM, m being an integer greater than or equal to one, the EEPROM outputs the collective verify signal for each page of data written into the [*31] EEPROM.

For the most part, the parties agree about the proper construction of this claim phrase. The remaining dispute here lies in whether the construction should explain from where and to where the signal is outputted (i.e. whether the construction should include Lexar's proposed "from the input/output buffer" language). Toshiba argues that Lexar's focus on defining the means for outputting a collective verify signal is redundant because surrounding claim language explains what generates the signal and what receives it. Lexar contends that including such language would be beneficial to the jury to understand exactly what the collective verify signal does. However, at oral argument, Lexar agreed that the Court could "properly construe th[e] term without . . . including an output from the input/output buffer." (Claim Construction Transcript at 31:14–22.) Therefore, the Court declines to incorporate from whence the collective verify signal is output in its construction of the claim phrase. To do so would improperly load up surrounding claim language into the construction of a single phrase.

"Collective verify signal" is construed as *a signal generated upon a simultaneous* [*32] *verification of the state of a plurality of memory cells.*

VII. "control unit" in the *231 patent*

Lexar's proposed compromise construction:	Toshiba's proposed compromise construction:
a circuit or group of circuits for interfacing with a memory	a circuit or group of circuits for interfacing with a memory

In their papers, the parties maintained that there was a dispute as to the construction of "control unit." Lexar proposed that the term should be construed as "a circuit or logical group of circuits for interfacing with a memory" or "an interface for a memory" while Toshiba proposed "a circuit for interfacing with a memory." At oral argument., the parties declared that they had come to an agreement with respect to the construction of "control unit." Toshiba agreed to add "or group of circuits" and Lexar agreed to drop "logical" from its proposed construction. Therefore, in alignment with the parties' agreed–upon proposed construction, "control unit" is construed as *a circuit or group of circuits for interfacing with a memory.*

VIII. "memory controller" in the *850/'104 patent*

Lexar's proposed construction:	Toshiba's proposed construction:
a circuit or group of circuits for interfacing with a memory	a circuit or group of circuits for interfacing with a memory

[*33]

As with "control unit" in the *231*, discussed *supra*, the parties described a dispute as to the construction of "memory controller" in the *850/' 104* in their papers, but informed the Court at oral argument that they had since reached an agreement. Toshiba initially proposed that "memory controller" should be construed as "a circuit or logical group of circuits for interfacing with a memory" or "an interface for a memory" while Toshiba proposed "a circuit for interfacing with a memory." n4 Toshiba has agreed to add "or group of circuits" and Lexar has agreed to drop "logical" from its proposed construction. The Court therefore construes "memory controller" as *a circuit or group of circuits for interfacing with a memory.*

n4 The parties have always agreed that "control unit" and memory controller" should have an identical construction.

IX. "memory means" in the *351 patent*

Corresponding structure according to Lexar:	Corresponding structure according to Toshiba:
memory cell array; bitline control circuit; row decoder; column decoder; address buffer; substrate potential control circuit; program completion detection circuit; input/output buffer	memory cell array, bitline control circuit

[*34]

Claim 1 of the *351* teaches a "memory means having a plurality of memory cells, for latching a data group composed of a predetermined number of bits transferred from a data register, for writing the latched data group in the memory cells, and for outputting a collective verify signal when all the data of the data group have been written." The parties agree that "memory means" in the *351* is a *section 112(6)* term and agree that the memory means performs three functions: latching a data group, writing the latched data group in the memory cells, and outputting a collective verify signal when all the data of the data group have been written. The parties even agree that the bitline control circuit is the structure that performs the latching and writing functions. Lexar and Toshiba only dispute whether the structure that performs the outputting function is limited to the bitline control circuit and the memory cell array or whether, as Lexar contends, other structures are required.

Toshiba, focusing on the claim language independent of the disclosed preferred embodiments, contends that the only corresponding structures necessary for performing the outputting function are the memory array [*35] and the bit line circuit. Lexar, however, argues that the corresponding structure must additionally six structures — the row decoder, the column decoder, the address buffer, the substrate potential control circuit, and most importantly, the program completion detection circuit and the input/output buffer. At oral argument, Toshiba expressed agreement that the program completion detection circuit and the input/output buffer have a role as "alternative elements." The debate, then, is whether the four other structures proposed by Lexar are necessary structures.

In identifying the corresponding structure set forth in the written description that performs the particular function set forth in the claim, the Court must not "permit incorporation of structure from the written description beyond that necessary to perform the claimed function." *Micro Chem., Inc. v. Great Plains Chem. Co., 194 F.3d 1250, 1257-58 (Fed. Cir. 1999)*. "Structural features that do not actually perform the recited function do not constitute corresponding structure and thus do not serve as serve as claim limitations." *Asyst Techs., Inc. v. Empak, Inc., 268 F.3d 1364, 1370 (Fed. Cir. 2001)*; [*36] *see also B. Braun Medical v. Abbott Lab., 124 F.3d 1419, 1424 (Fed. Cir. 1997)*. The question, here, is whether the corresponding structures identified by Lexar are all clearly linked or associated to the outputting function of the memory means. *Kahn v. GMC, 135 F.3d 1472, 1476 (Fed. Cir. 1998)*. If not, they cannot serve to limit the means-plus-function claim.

Lexar contends that all of the structures it identifies are necessary for performing the outputting function. However, neither in its brief nor at oral argument did Lexar provide argument, except in a footnote, to explain why four of its proposed structures — the row decoder, the column decoder, the address buffer, the substrate potential control circuit — are necessary corresponding structure. The Court finds that nothing in the patent suggests that these structures are directly related to the latching, writing, and outputting functions of the memory means. Therefore, the corresponding structure for "memory means" in the *351* is *the memory cell array, the bitline control circuit, the program completion detection circuit, and the input/output buffer.*

X. "memory [*37] means" in the *067 patent*

Corresponding structure according to Lexar:	Corresponding structure according to Toshiba:
EEPROM module (Fig. 1)	EEPROM (Fig. 1 and 11)

Claim 1 of the *067* recites a "memory means having a memory cell array divided into a plurality of blocks." Claim 16 recites a "memory means having a memory cell array divided into a plurality of blocks including unused blocks." The parties agree that this is a means-plus-function claim and they agree that the corresponding structure is not the same as the corresponding structure to the "memory means" claim in the *351*. The parties even agree that the corresponding structure to the "memory means" in the *067* is EEPROM, as depicted in Figure 1 in the specification, showing an EEPROM module, is corresponding structure. Toshiba contends, however, that Figure 11, depicting the arrangement of storage areas of the EEPROM in a second embodiment, is also corresponding structure. The Court disagrees.

Although Figure 11 is described in the *067* specification as "a memory means," nothing in the specification indicates that Figure 11, depicting the arrangement of storage areas in an EEPROM, is adequately linked [*38] to the function of the means element. Nor is there any indication that the structure represented in Figure 11 can perform the functions claimed by the memory means. Toshiba suggests that if Figure 11 is not corresponding structure, neither is Figure 1 because they are described identically. However, Toshiba misses that the description of Figure 11, at column 9, lines 23-40, in fact explains that the figure merely depicts "the arrangement of storage areas in an EEPROM" and that it is the EEPROM that "serv[es] as a memory means." Figure 11, as Lexar argues, is a stylized rendering of six units of storage. The Court finds that the corresponding structure to the "memory means" in the *067* is EEPROM as represented by Figure 1.

XI. "erasing means" in the *067 patent*

Corresponding structure according to Lexar:	Corresponding structure according to Toshiba:
CPU and algorithm being run in CPU and control logic	CPU programmed as disclosed in the specification to perform the functions of control means recited in the claim

Claim 1 of the *067* recites "erasing means for discriminating said erased blocks of said unused blocks from said non-erased blocks of said [*39] unused blocks and erasing data stored in said non-erased blocks." The parties agree that "erasing means" is a means-plus-function limitation. They also agree that the central processing unit ("CPU") is at least part of the corresponding structure of the erasing means. But Lexar argues that the structure must also include the algorithm for performing the function and Toshiba contends that Lexar's proposed construction is so broad as to impermissibly import an unclaimed functionality into the structure.

While Toshiba initially argued that a CPU was the proper corresponding structure, it amended its argument to identify a CPU "programmed as disclosed in the specification to perform the [discriminating and erasing data] functions of erasing means recited in the claim." This is very close to Lexar's proposed "CPU and algorithm being run in CPU." However, for the following reasons, the Court finds Lexar's proposed structure more compelling.

The *067* specification discloses that CPU 14, in Figure 1, functions as erasing means. (Col. 5, lines 21-22.) Lexar contends that the structure of Figures 8A and 8B or any structure described in lines 38-45 of column 8 of the specification is also [*40] corresponding structure. The Court agrees. A generic CPU is too broad to be the corresponding structure, as Lexar contends. *See e.g., WMS Gaming Inc. v. Int'l Game Tech., 184 F.3d 1339 (Fed. Cir. 1999)*. The algorithm executed by a computer claimed in a means-plus-function claim is part of the corresponding structure. *Id.* To identify only the CPU as corresponding structure would improperly broaden the means-plus-function claim. Toshiba's compromise does not solve this problem because "programmed as disclosed in the specification to perform the functions of the erasing means recited in the claim" is so vague as to add nothing meaningful to the discussion. Therefore, the Court finds that the corresponding structure for "erasing means" in the *067* is *CPU and algorithm being run in CPU, as described in Figures 8A and 8B; D1, D6, and D10.*

XII. "control means" in the *067 patent*

Corresponding structure according to Lexar:	Corresponding structure according to Toshiba:
CPU and algorithm being run in CPU and control logic	CPU programmed as disclosed in the specification to perform the functions of control means recited in the claim

[*41]

A "control means" is recited in independent claims 1 and 16 of the *067*. Although claims 1 and 16 recite different functions for the control means, the parties agree that the corresponding structure is the same for the recited "control means" claims. The parties agree that the CPU is corresponding structure. The *067* specification discloses that CPU 14, in Figure 1, functions as control means. (Col. 5, lines 21-22.) But Lexar urges the Court to find, consistent with the Federal Circuit's holding in the *WMS Gaming* case, that the algorithm being run in CPU is also part of the corresponding structure as is "control logic." *184 F.3d 1339*. Toshiba again proposes a compromise corresponding structure so as not to import additional functionality into the structure by including the entire algorithm and Toshiba rejects "control logic" as corresponding structure.

The algorithm dispute is the same as the one in discussed for "erasing means" *supra.* A generic CPU is too broad to be the corresponding structure; the algorithm executed by a computer claimed in a means-plus-function claim is part of the corresponding structure. *WMS Gaming Inc., 184 F.3d 1339.* [*42] Therefore, again, the Court finds that the CPU's algorithm must be included in the corresponding structure of the functions performed by the "control means."

Lexar also proposes to include "control logic circuit 11" as structure that corresponds to the functions of "control means" recited in claims 1 and 16. The *067* specification discloses that the control logic circuit transfers and writes data to the EEPROM. (Column 8, lines 54-60.) Toshiba contends, however, that the control logic circuit is not necessary structure and that the CPU, as the control means, controls several structural elements, including the control circuit logic, but that that does not render those structure elements corresponding structure. For example, the CPU finds a block in which to write the data and communicates with a data buffer, but neither said block or said data buffer are part of the corresponding structure. The Court sees no real distinction between these types of structural elements with which the CPU interacts and the control logic circuit and finds, therefore, that the control logic circuit is not necessary corresponding structure for performing the "control means." The corresponding structure for [*43] "control means" is *CPU and algorithm being run in CPU.*

XIII. "managing means" in the *067 patent*

Corresponding structure according to Lexar:	Corresponding structure according to Toshiba:
management table (Figs. 2 and 3)	management table (Fig. 2)

The parties agree that the management table (Figure 2), disclosed in the specification as the structure that corresponds to the "managing means" means-plus-function claim in the *067*, but they disagree as to whether the corresponding structure must also encompass Figure 3. Lexar urges a narrower construction here, arguing that Figure 3 is also corresponding structure, while Toshiba contends that Figure 2 is all the structure that is necessary to perform the managing means functionality.

In claim 1, the "managing means" has the functionality of "managing unused blocks of said plurality of blocks in which new data is to be written." Toshiba argues that Figures 3A-3C are not necessary to accomplish the managing means function recited in claim 1 and that to identify Figures 3A-3C as part of the corresponding structure would improperly import unnecessary structure into a claim. The Court agrees.

Figures 3A-3C [*44] do depict operations for managing unused blocks; that is, they can perform the functions recited in claim 1 for managing means. However, the language of the patent specification suggests that these drawings are merely examples of a management table's operations and are not part of the corresponding structure. At column 5, lines 66-67, immediately following a four-paragraph description of the management table as depicted in Figure 2 (and a variation in Figure 4), the following language appears: "An operation of recording data will be briefly described below using practical examples." Then the processes depicted in Figures 3A-3C are described. These are examples of management table operations, not necessary structure for performing the managing means functionality. Therefore, the Court finds that the *management table* (Figure 2) is the corresponding structure for the "managing means." Figure 3 is not corresponding structure.

XIV. "means for informing" in the *067 patent*

Corresponding structure according to Lexar:	Corresponding structure according to Toshiba:
CPU and erase flag of Fig. 2	CPU programmed as disclosed in the specification to

Corresponding structure according to Lexar:	Corresponding structure according to Toshiba: perform the functions of the means for informing recited in the claim.

[*45]

Claim 6 of the *067* recites that "said erasing means includes means for informing said managing means that data of a non–erased block has been erased when the data of said non–erased block is erased by said erasing means." Lexar and Toshiba agree that this is a means–plus–function limitation, that the means for informing is part of the erasing means, and that the CPU is corresponding structure. But Lexar contends that the erase flag of Figure 2 is also part of the corresponding structure, while Toshiba disagrees.

The CPU, along with the CPU's algorithm, is the structure that corresponds to the erasing means functionality. Because the "means for informing" is, as both parties acknowledge, part of the erasing means, the structure is the same. The corresponding structure for "means for informing" in the *067* is *CPU and algorithm being run in CPU.*

CONCLUSION

For the foregoing reasons, the Court construes the disputed claim terms as follows:

1. "page" in the *351* and *696 patents* is construed as *the unit of data, consisting of a plurality of bytes, programmed to and read from the memory at the same time.*

2. "page" in the *933 patent* is construed as *the unit* [*46] *of data, consisting of a plurality of bytes, written to and read from the memory at the same time.*

3. "order" in the *067 patent* is construed as *a logical or comprehensible arrangement of unused blocks.*

4. "simultaneously" in the *351/'696 patent* is construed as *at the same time.*

5. "simultaneously" in the *933 patent* is construed as *at the same time.*

6. "collective verify signal" in the *351 patent* is construed as *a signal generated upon a simultaneous verification of the state of a plurality of memory cells.*

7. "control unit" in the *231 patent* is construed as *a circuit or group of circuits for interfacing with a memory.*

8. "memory controller" in the *850/' 104 patents* is construed as *a circuit or group of circuits for interfacing with a memory.*

9. The corresponding structure for the "memory means" means–plus–function claim in the *351 patent* is *the memory cell array, the bitline control circuit, the program completion detection circuit, and the input/output buffer.*

10. The corresponding structure for the "memory means" means–plus–function claim in the *067 patent* is *EEPROM module (Figure 1).*

11. The corresponding [*47] structure for the "erasing means" means–plus–function claim in the *067 patent* is *CPU and algorithm being run in CPU, as described in Figures 8A & 8B; D1, D6, and D10.*

12. The corresponding structure for the "control means" means–plus–function claim in the *067 patent* is *CPU and algorithm being run in CPU.*

13. The corresponding structure for the "managing means" means–plus–function claim in the *067 patent* is *management table (Figure 2)*; and

14. The corresponding structure for the "means for informing" means–plus–function claim in the *067 patent* is *CPU and algorithm being run in CPU.*

IT IS SO ORDERED.

Dated: January 24, 2005

MARTIN J. JENKINS

UNITED STATES DISTRICT JUDGE